INTL9555 Product Brief

1. Description

This chip is a 24-pin CMOS device that provides 16 bits of general-purpose parallel input/output (GPIO) expansion for I2C-bus/SMBus applications. The INTL9555 has high drive capability,5V I/O tolerance,lower supply current,individual I/O configuration and smaller packaging.I/O expanders provide a simple solution when additional I/O is needed.

This 16-bit I/O expander for the two-line bidirectional bus (I2C) is designed for 1.65V to 5.5V VCC operation. It provides general-purpose remote I/O expansion for most microcontroller families via the I2C interface. This chip consists of two 8-bit configuration (input or output selection), input port, output port, and polarity inversion registers. At power on, the I/Os are configured as inputs. The system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding Input or output register. The polarity of the Input port register can be inverted with the polarity inversion register.

2. Applications

- IT infrastructure (servers, storages)
- 5g communication
- Network system, including switches and routers

3. Key Features

- The operating power supply voltage range of 1.65V to 5.5V
- 5V tolerant I/Os
- Polarity inversion register
- Active low interrupt output
- Low standby current
- Noise filter on SCL/SDA inputs
- Internal power-on reset
- No glitch on power-up
- 16 I/O pins which default to 16 inputs
- 0 Hz to 400 kHz clock frequency
- The package is TSSOP-24

4. Functional Diagram

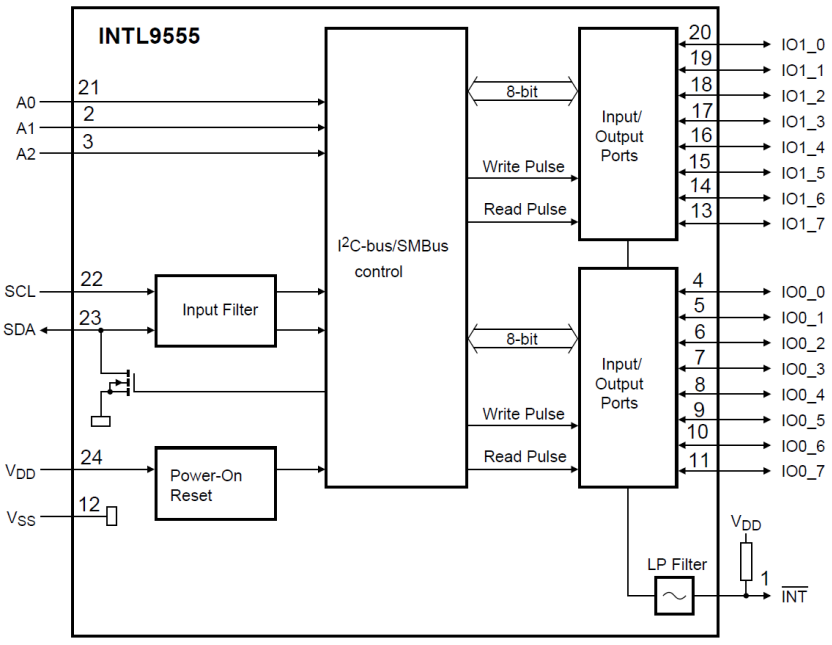

Figure 1 Functional Diagram

5. Pin Maps

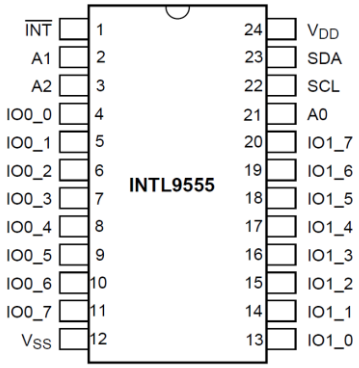

Figure 2 Pin Assignment Diagram- TSSOP-24

6. Pin Descriptions

Table 1 Pin Descriptions

Name	Pin Number	Description
$\overline{INT}$	1	Interrupt output. Connect to V_{CC} through a pullup resistor.
A1	2	Address input 1. Connect directly to V_{CC} or ground.
A2	3	Address input 2. Connect directly to V_{CC} or ground.
IO0_0	4	P-port input/output. Push-pull design structure.
IO0_1	5	P-port input/output. Push-pull design structure.
IO0_2	6	P-port input/output. Push-pull design structure.
IO0_3	7	P-port input/output. Push-pull design structure.
IO0_4	8	P-port input/output. Push-pull design structure.
IO0_5	9	P-port input/output. Push-pull design structure.
IO0_6	10	P-port input/output. Push-pull design structure.
IO0_7	11	P-port input/output. Push-pull design structure.
VSS	12	Ground
IO1_0	13	P-port input/output. Push-pull design structure.
IO1_1	14	P-port input/output. Push-pull design structure.
IO1_2	15	P-port input/output. Push-pull design structure.
IO1_3	16	P-port input/output. Push-pull design structure.
IO1_4	17	P-port input/output. Push-pull design structure.
IO1_5	18	P-port input/output. Push-pull design structure.
IO1_6	19	P-port input/output. Push-pull design structure.
IO1_7	20	P-port input/output. Push-pull design structure.
A0	21	Address input 0. Connect directly to V_{CC} or ground.
SCL	22	Serial clock bus. Connect to V_{CC} through a pullup resistor.
SDA	23	Serial data bus. Connect to V_{CC} through a pullup resistor.
VDD	24	Supply voltage