INTL9554 Product Brief

1. Description

The INTL9554 are 16-pin CMOS devices that provide 8 bits of General Purpose parallel Input/Output (GPIO) expansion for I2C-bus/SMBus applications.

The improvements include higher drive capability, 5 V I/O tolerance, lower supply current, individual I/O configuration, 400 kHz clock frequency, and smaller packaging. I/O expanders provide a simple solution when additional I/O is needed for ACPI power switches, sensors, push buttons, LEDs, fans, and so on.

The INTL9554 consist of an 8-bit Configuration register (Input or Output selection); 8-bit Input Port register, 8-bit Output Port register and an 8-bit Polarity Inversion register (active HIGH or active LOW operation). The system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding Input Port or Output Port register. The polarity of the read register can be inverted with the Polarity Inversion register. All registers can be read by the system master.

The INTL9554 open-drain interrupt output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed. The power-on reset sets the registers to their default values and initializes the device state machine.

Three hardware pins (A0, A1, A2) vary the fixed I2C-bus address and allow up to eight devices to share the same I2C-bus/SMBus.

2. Applications

- Servers
- Routers (Telecom Switching Equipment)
- Factory Automation
- Products With I2C Slave Address Conflicts

3. Key Features

- Operating power supply voltage range of 1.65 V to 5.5 V
- 5 V tolerant I/Os
- Polarity Inversion register
- Active LOW interrupt output
- Low standby current
- Noise filter on SCL/SDA inputs
- No glitch on power-up
- Internal power-on reset
- 8 I/O pins which default to 8 inputs
- 0 Hz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- AEC-Q100 compliance available
- Packages offered: TSSOP16

4. Functional Diagram

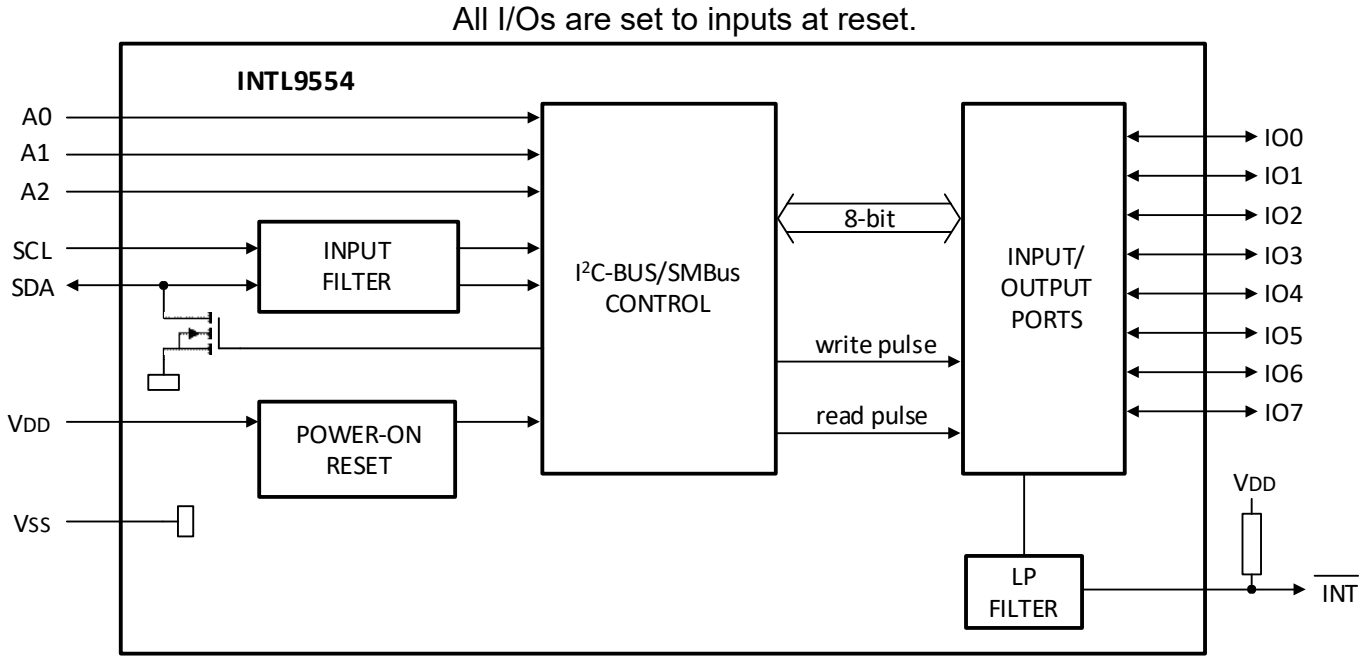

Figure 1 Functional Diagram

5. Pin Maps

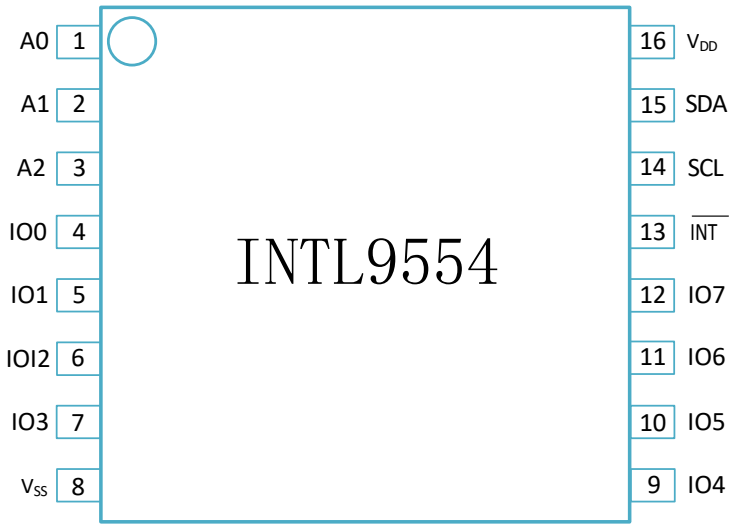

Figure 2 Pin Assignment Diagram

6. Pin Descriptions

Table 1 Pin Descriptions

Symbol	Pin	Description
A0	1	address input 0
A1	2	address input 1
A2	3	address input 2

IO0	4	Input/output 0
IO1	5	Input/output 1
IO2	6	Input/output 2
IO3	7	Input/output 3
VSS	8	Input/output 4
IO4	9	Input/output 4
IO5	10	Input/output 5
IO6	11	Input/output 6
IO7	12	Input/output 7
$\overline{INT}$	13	Interrupt output(open-drain)
SCL	14	serial clock line
SDA	15	serial data line
VDD	16	supply voltage